# NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

## RELATED APPLICATIONS

**[0001]** This application is the U.S. National Phase under 35 U.S.C. §371 of International Application No. PCT/JP2008/002992, filed on Oct. 22, 2008, which in turn claims the benefit of Japanese Application No. 2007-281181, filed on Oct. 30, 2007, the disclosures of which Applications are incorporated by reference herein.

## TECHNICAL FIELD

**[0002]** The present invention relates to a cross-point nonvolatile semiconductor memory device using a resistance variable layer. Particularly, the present invention relates to a configuration of a lead-out contact in a configuration in which a diode is integrated into a wire layer.

## BACKGROUND ART

**[0003]** In recent years, with advancement of digital technologies of electronic hardware, semiconductor memory devices which have a large capacity and are nonvolatile have been developed vigorously to store data of music, image, information and so on. For example, a nonvolatile semiconductor memory device using a ferroelectric as a capacitive element has been already used in many fields. In addition to the nonvolatile memory device using such a ferroelectric capacitor, a nonvolatile semiconductor memory device (hereinafter referred to as ReRAM) using a material which is adapted to switch a resistance value in response to electric pulses applied and retains the state has attracted an attention because of its high compatibility with a standard semiconductor process.

**[0004]** For example, there is disclosed a device configuration of a ReRAM including one transistor and one memory section, for enabling the use of the existing DRAM based process as it is (see, for example, Patent document 1). The ReRAM includes a transistor and a nonvolatile memory section connected to a drain of the transistor. The memory section has a structure in which a resistance variable layer switching resistance reversibly in response to current pulses is sandwiched between an upper electrode and a lower electrode. As the resistance variable layer, a nickel oxide layer (NiO), a vanadium oxide layer ($V_2O_5$), a zinc oxide layer (ZnO), a niobium oxide layer ($Nb_2O_5$), a titanium oxide layer ($TiO_2$), a tungsten oxide layer ($WO_3$), a cobalt oxide layer (CoO), etc are used. It is known that such transition metal oxide layers exhibit a specified resistance value upon application of a voltage or current which is not lower than a threshold and retains the resistance value until a voltage or current is newly applied thereto. In addition, such the transition metal oxide layers have a feature that it can be manufactured using the existing DRAM based process as it is.

**[0005]** The above mentioned example has a configuration including one transistor and one nonvolatile memory section. A cross-point ReRAM using a perovskite structure material is disclosed (see, for example, patent document 2). In this ReRAM, stripe-shaped lower electrodes are formed on a substrate and an active layer is formed over the entire surface to cover the lower electrodes. As the active layer, a resistance variable layer which switches resistance reversibly in response to electric pulses is used. On the active layer, stripe-shaped upper electrodes are formed to respectively cross the lower electrodes such that the upper electrodes are perpendicular to the lower electrodes. A region where the lower electrode crosses the upper electrode with the active layer sandwiched between them is a memory section. Each of the lower electrode and the upper electrode serves as either a word line or a bit line. It is disclosed that such a cross-point configuration can achieve a larger capacity.

**[0006]** In the cross-point ReRAM, a diode is incorporated to be arranged in series with a resistance variable layer to avoid an influence of resistance variable layers belonging to other rows and columns, when reading a resistance value of the resistance variable layer formed at a cross point.

**[0007]** For example, a ReRAM is disclosed, comprising a substrate including two or more bit lines arranged in parallel with each other, two or more word lines which are arranged in parallel with each other so as to respectively cross the bit lines, resistive structures formed on the bit lines at positions where the bit lines respectively cross the word lines, and diode structures formed on the resistive structures in contact with the resistive structures and the word lines, lower electrodes formed on the substrate, resistive structures formed on the lower electrodes, diode structures formed on the resistive structures, and upper electrodes formed on the diode structures (see Patent document 3).

**[0008]** In such a configuration, a unit cell structure can be formed to have a layer structure including a single diode structure and a single resistive structure which are stacked continuously, and an array cell structure is easily attained.

**[0009]** Also, a cross-point ReRAM is disclosed, in which memory plugs are formed at cross points where X-direction conductive array lines **210** respectively cross Y-direction conductive array lines **215** (see e.g., Patent document 4). In Patent document 4, as shown in FIG. **11**, the memory plug is composed of seven layers and contains therein a memory element **255** including a composite metal oxide **225** and two electrode layers **220** and **230** sandwiching the composite metal oxide **225**, and a non-ohmic element **260** which is formed on the memory element **255** and has a metal-insulator-metal (MIM) structure consisting of a metal layer **235**, an insulating layer **240** and a metal layer **245** which are stacked together such that the memory element **255** and the non-ohmic element **260** are provided via an electrode layer **250**.

**[0010]** Patent document 1: Japanese Laid-Open Patent Application Publication No. 2004-363604

**[0011]** Patent document 2: Japanese Laid-Open Patent Application Publication No. 2003-68984

**[0012]** Patent document 3: Japanese Laid-Open Patent Application Publication No. 2006-140489

**[0013]** Patent document 4: U.S. Pat. No. 6,753,561 Specification

## DISCLOSURE OF THE INVENTION

### Problems to be Solved by the Invention

**[0014]** Patent document 1 also discloses a structure of a single diode having a switching function and a single resistive element, but fails to disclose or suggest a specific structure of the resistive element and the diode. Patent document 2 discloses the cross-point configuration, but fails to disclose or suggest series connection of the diode or its specific structure, as in Patent document 1.

**[0015]** In contrast to the above, Patent document 3 discloses a configuration in which a resistive structure is formed